This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Cancelled).

2. (Currently Amended) A memory system as recited in claim 6 ~~claim 1~~, wherein said storage elements are identical regardless of whether associated with the first portion or the second portion.

3. (Currently Amended) A memory system as recited in claim 6 ~~claim 1~~, wherein said storage elements are provided on a common substrate.

4. (Currently Amended) A memory system as recited in claim 6 ~~claim 1~~, wherein said memory system is provided within a single portable semiconductor memory product.

5. (Currently Amended) A memory system ~~as recited in claim 1~~ that couples to a host, said memory system comprising:

a plurality of storage elements, a first portion of said storage elements for providing low density storage, and a second portion of said storage elements for providing high density storage; and

a controller operatively connected to said storage elements, said controller operates to receive commands for data access from the host and to control reading and writing of data into said storage elements in accordance with the commands,

wherein said storage elements configured for low density storage store one or two bits per cell, and wherein said storage elements configured for high density storage store four or more bits per cell.

6. (Currently Amended) A memory system ~~as recited in claim 1~~ that couples to a host, said memory system comprising:

a plurality of storage elements, a first portion of said storage elements for providing low density storage, and a second portion of said storage elements for providing high density storage; and

a controller operatively connected to said storage elements, said controller operates to receive commands for data access from the host and to control reading and writing of data into said storage elements in accordance with the commands,

wherein said storage elements are non-volatile storage elements.

7. (Currently Amended) A memory system ~~as recited in claim 1~~ that couples to a host, said memory system comprising:

a plurality of storage elements, a first portion of said storage elements for providing low density storage, and a second portion of said storage elements for providing high density storage; and

a controller operatively connected to said storage elements, said controller operates to receive commands for data access from the host and to control reading and writing of data into said storage elements in accordance with the commands,

wherein said storage elements are Flash type storage elements.

8. (Currently Amended) A memory system ~~as recited in claim 1~~ that couples to a host, said memory system comprising:

a plurality of storage elements, a first portion of said storage elements for providing low density storage, and a second portion of said storage elements for providing high density storage; and

a controller operatively connected to said storage elements, said controller operates to receive commands for data access from the host and to control reading and writing of data into said storage elements in accordance with the commands,

wherein said storage elements configured for low density storage store one bit per cell, and wherein said storage elements configured for high density storage store two or more bits per cell.

9. (Currently Amended) A memory system as recited in claim 5 ~~claim 1~~, wherein said storage elements are Flash type storage elements.

10. (Currently Amended) A memory system as recited in claim 5 ~~claim 1~~, wherein said storage elements are EEPROM type storage elements.

11. (Cancelled).

12. (Cancelled).

13. (Currently Amended) A hybrid memory device ~~as recited in claim 12,~~ having a single substrate, said hybrid memory device comprising:

a plurality of low density storage elements;

a plurality of high density storage elements; and

a controller operatively connected to said low density storage elements and said high density storage elements, said controller operates to control read, write and erasure of data into said low density storage elements and said high density storage elements,

wherein said low density storage elements and said high density storage elements are memory cells, and

wherein said low density storage elements store one or two bits per cell, and wherein said high density storage elements store four or more bits per cell.

14. (Currently Amended) A hybrid memory device ~~as recited in claim 12,~~ having a single substrate, said hybrid memory device comprising:

a plurality of low density storage elements;

a plurality of high density storage elements; and

a controller operatively connected to said low density storage elements and said high density storage elements, said controller operates to control read, write and erasure of data into said low density storage elements and said high density storage elements,

wherein said low density storage elements and said high density storage elements are memory cells, and

wherein said low density storage elements store two bits per cell, and wherein said high density storage elements store four bits per cell.

15. (Currently Amended) A hybrid memory device ~~as recited in claim 11,~~ having a single substrate, said hybrid memory device comprising:

a plurality of low density storage elements;

a plurality of high density storage elements; and

a controller operatively connected to said low density storage elements and said high density storage elements, said controller operates to control read, write and erasure of data into said low density storage elements and said high density storage elements,

wherein said low density storage elements and said high density storage elements are Flash type storage elements or EEPROM type storage elements.

16. (Cancelled).

17. (Currently Amended) A hybrid memory device as recited in claim 13 ~~claim 11~~, wherein said low density storage elements and said high density storage elements have a common device structure.

18. (Original) A hybrid memory device as recited in claim 17, wherein data stored to said low density storage elements can be read in substantially less time than it takes to read data from said high density storage elements.

19. (Currently Amended) A hybrid memory device ~~as recited in claim 18,~~ having a single substrate, said hybrid memory device comprising:

a plurality of low density storage elements;

a plurality of high density storage elements; and

a controller operatively connected to said low density storage elements and said high density storage elements, said controller operates to control read, write and erasure of data into said low density storage elements and said high density storage elements,

wherein said low density storage elements and said high density storage elements have a common device structure,

wherein data stored to said low density storage elements can be read in substantially less time than it takes to read data from said high density storage elements, and

wherein the common device structure is a Flash device structure.

20. (Currently Amended) A hybrid memory device ~~as recited in claim 18,~~ having a single substrate, said hybrid memory device comprising:

a plurality of low density storage elements;

a plurality of high density storage elements; and

a controller operatively connected to said low density storage elements and said high density storage elements, said controller operates to control read, write and erasure of data into said low density storage elements and said high density storage elements,

wherein said low density storage elements and said high density storage elements have a common device structure,

wherein data stored to said low density storage elements can be read in substantially less time than it takes to read data from said high density storage elements, and

wherein said hybrid memory device is a portable memory card having non-volatile memory, and

wherein said low density storage elements and said high density storage elements are non-volatile storage elements.

21-33. (Cancelled).

34. (Withdrawn) A method as recited in claim 33, wherein the data storage elements are non-volatile.

35. (Withdrawn) A method as recited in claim 34, wherein the data storage elements operate in a low density storage mode and a high density storage mode.

36. (Withdrawn) A method as recited in claim 35, wherein the memory product further includes volatile storage, and wherein the address translation table is stored in the volatile storage.